United States Patent Office 2,846,142 Patented Aug. 5, 1958

2,846,142

ELECTRONIC DIGITAL COMPUTING ENGINES

Christopher Strachey, London, England, and Donald Bruce Gillies, Toronto, Ontario, Canada, assignors to National Research Development Corporation, London, England, a British corporation

Application August 25, 1954, Serial No. 452,026

Claims priority, application Great Britain August 27, 1953

10 Claims. (Cl. 235—61)

The present invention relates to electronic digital computing machines. In the specifications of copending patent applications Nos. 418,104, 418,105 and 418,129 there is described a computing machine in which information is stored in delay lines in dynamic, serial form in some parts of the machine and in the form of magnetic recordings on a rotating disc, which forms the main information store of the machine. The present invention is primarily concerned with apparatus for performing the function of multiplication and will be described in relation to the machine to which the above mentioned patent applications relate, as constituting a modified form of part of the arithmetic organ of that machine. It will be understood, however, that the present invention may be applied to other types of machine.

In performing the process of multiplication, as is well-known, the multiplication of two numbers results in a product having twice as many digits as either of the original numbers so that if, as is normally the case, the storage facilities of a machine comprise registers each adapted to accommodate the digits of a single so-called "word" it is necessary to combine two such registers or provide a special double-length register to accommodate the double-length word resulting from a multiplication. In the machine above referred to multiplication is effected using two single word registers in tandem for the product of a multiplication; the multiplication process consists in performing a series of additions in which the multiplicand, shifted by the appropriate number of digit positions is added to itself (or an existing partial product) or not according to whether or not the multiplier contains "1" in the relevant digit position and this process is achieved by circulating the multiplicand (or the partial product) through the two registers in series, effecting a shift of one digit position at each circulation, the multiplicand being added in at the appropriate time in the circulation cycle under control of the multiplier. Initially the multiplier may be stored in one of the series-connected registers, it being "lost" digit-by-digit as the multiplication proceeds, the digits of the multiplier being discarded as they are used and the storage space thus liberated being employed to accommodate the growing partial product. It will be appreciated that with such an arrangement the double-length register formed by the two word-length registers in series will require two word times for each circulation of its contents.

One object of the present invention is to provide an arrangement which will enable the process of multiplication to be carried out more rapidly in such a machine.

According to this invention in one aspect therefore an arrangement is provided for effecting multiplication in an electronic digital computer comprising circulating delay line storage registers, the multiplying arrangement comprising three such registers each of one word length and each provided with its own circulation loop, an adding circuit connected in the circulation loop of one of said registers (accumulator register) a gate circuit connected between another of said registers (multiplicand register) and said adding circuit means for controlling said gate circuit said means comprising a control circuit connected between the third of said registers (multiplier register) and said gate circuit and a transfer circuit connected between said accumulator register and said multiplier register for transferring digit signals from said accumulator to said multiplier register. Said accumulator and multiplier registers are preferably of different length from the multiplicand register by one digit time, whereby the numbers circulating in them are shifted by one digit with respect to the number in the multiplicand register for each circulation of the registers.

It will thus be seen that a digit of the multiplier will be employed at each word time to set up said control circuit and will control (by whether it is a "0" or a "1") whether or not the multiplicand is fed through the adding gate into the accumulator register and added to the contents thereof. Each such addition will take place with a shift relative to the contents of the accumulator register appropriate to the significance of the multiplier digit which caused the addition to be made, as is required for the multiplication process. The contents of the accumulator register is, therefore, the partial product, which will grow digit-by-digit as the multiplier digits are used up and these additional digits will be transferred to the multiplier register by the transfer gate to refill the digit intervals vacated by the multiplier digits which have been used. These transferred digits will be circulated with the multiplier digits. When the multiplication is complete the double-length word representing the product will thus be contained as to one half in the accumulator register (in general the most significant half) and as to the other half in the multipler register where it replaces the multiplier.

It will be appreciated that by using an arrangement as above described, each stage of the multiplication occupies only one word time as against two word times in the known arrangements above mentioned.

The above discussion does not take account of the sign of the numbers being multiplied or of the product. In binary arithmetic as practised in machines of the kind to which this invention relates, the sign of a number is indicated by the digit in the position of greatest significance. This digit is a "0" for positive numbers or a "1" for negative numbers. The logic of this arrangement derives from the convention that all the numbers manipulated in the machine are regarded as lying between $+1$ and -1. It follows that if we subtract 2 from a positive number which is less than 1 a negative resultant is obtained and the presence of a "1" in the digit position of greatest significance indicates that this subtraction must be made and a negative number is thus implied. In the process of multiplication the significance of a "1" in the "sign digit" position of the multiplier is that the last operation must be the subtraction of the multiplicand from the partial product in the position of greatest significance instead of addition as in the previous stages.

The present invention has for a further object the provision of means for complying with this requirement.

According to the invention in this aspect there is provided a multiplier for electronic digital computing machines in which instruction words contain two addresses related to information stored in a storage facility of the machine, and in which the machine is invested with one operative condition while searching for one of said addresses in an instruction word and with a different operative condition while searching for the other of said addresses, said multiplier including a gate circuit adapted to effect addition of a multiplicand to a partial product in the normal process of multiplication and being adapted to be converted to perform the function of sub-